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Abstract
A sigma-delta codec(SDC) including four main blocks, a sigma-delta modulator(SDM), a decimator, an interpolator, and a sigma-delta demodulator(SDDM) is presented. In order to achieve low-voltage and low-power issues, a novel class AB switched-current(SI) integrator is used to implement the SDM, which has the oversampling ratio(OSR) of 64. Benefits of the SDM using the class AB SI integrator are low-voltage, low-power consumption, high linearity, and high dynamic range.

In addition, the decimator and interpolator consist of a fourth-order comb filter, two FIR filters, and a compensation filter, the proposed single-multiplier structure is applied to the finite impulse response(FIR) filters of the decimator and the interpolator which both of them share the common hardware in the implementation. Therefore, the number of multipliers and chip area are reduced.

The whole codec was implemented using a TSMC 0.35μm 2P4M Mixed-mode process technology. Simulation results according to a sinusoidal wave input of 1kHz with 4kHz bandwidth show that the codec has a maximum signal-to-noise and distortion ratio(SNDR) and dynamic range over 54dB at the output of the SDC with a single 2.5V power supply.
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